

### Description

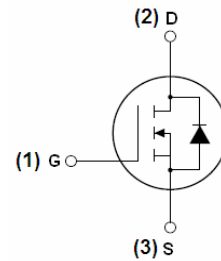
The HM25N06Q uses advanced trench technology and design to provide excellent  $R_{DS(ON)}$  with low gate charge. It can be used in a wide variety of applications.

### General Features

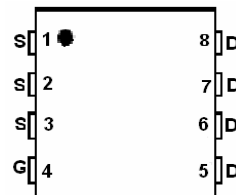
- $V_{DS} > 60V, I_D = 25A$   
 $R_{DS(ON)} < 20m\Omega @ V_{GS}=10V$  (Typ:18m $\Omega$ )
- High density cell design for ultra low  $R_{dson}$
- Fully characterized avalanche voltage and current
- Low gate to drain charge to reduce switching losses

### Application

- Power switching application
- Hard switched and high frequency circuits
- Uninterruptible power supply



Schematic diagram



Marking and pin assignment

### Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
HM25N06Q	HM25N06Q	DFN3X3-8L	--	--	--

### Absolute Maximum Ratings ( $T_A=25^\circ C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DS}$	60	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Drain Current-Continuous	$I_D$	25	A
Drain Current-Continuous( $T_C=100^\circ C$ )	$I_D(100^\circ C)$	17	A
Pulsed Drain Current	$I_{DM}$	85	A
Maximum Power Dissipation	$P_D$	40	W
Operating Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 To 150	$^\circ C$

### Thermal Characteristic

Thermal Resistance, Junction-to-Ambient <sup>(Note 2)</sup>	$R_{\theta JA}$	3.75	$^\circ C/W$
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### Electrical Characteristics ( $T_A=25^\circ C$ unless otherwise noted)

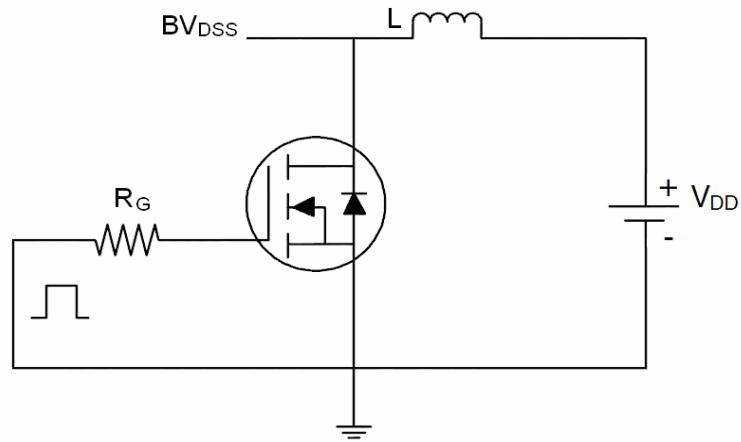
Parameter	Symbol	Condition	Min	Typ	Max	Unit
<b>Off Characteristics</b>						
Drain-Source Breakdown Voltage	BVDSS	V <sub>GS</sub> =0V, I <sub>D</sub> =250μA	60	69	-	V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =60V, V <sub>GS</sub> =0V	-	-	1	μA
Gate-Body Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> =±20V, V <sub>DS</sub> =0V	-	-	±100	nA
<b>On Characteristics</b> (Note 3)						
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250μA	1.2	2.0	2.5	V
Drain-Source On-State Resistance	R <sub>DS(ON)</sub>	V <sub>GS</sub> =10V, I <sub>D</sub> =5A		18	20	
Forward Transconductance	g <sub>FS</sub>	V <sub>DS</sub> =5V, I <sub>D</sub> =5A	11	-	-	S
<b>Dynamic Characteristics</b> (Note4)						
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> =30V, V <sub>GS</sub> =0V, F=1.0MHz		1000		PF
Output Capacitance	C <sub>oss</sub>			100		PF
Reverse Transfer Capacitance	C <sub>rss</sub>			67		PF
<b>Switching Characteristics</b> (Note 4)						
Turn-on Delay Time	t <sub>d(on)</sub>	V <sub>DS</sub> =30V, I <sub>D</sub> =5A, V <sub>GS</sub> =10V, R <sub>GEN</sub> =3Ω	-	4.7	-	nS
Turn-on Rise Time	t <sub>r</sub>		-	2.3	-	nS
Turn-Off Delay Time	t <sub>d(off)</sub>		-	15.7	-	nS
Turn-Off Fall Time	t <sub>f</sub>		-	1.9	-	nS
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> =30V, I <sub>D</sub> =5A, V <sub>GS</sub> =10V	-	30	-	nC
Gate-Source Charge	Q <sub>gs</sub>		-	10	-	nC
Gate-Drain Charge	Q <sub>gd</sub>		-	5	-	nC
<b>Drain-Source Diode Characteristics</b>						
Diode Forward Voltage (Note 3)	V <sub>SD</sub>	V <sub>GS</sub> =0V, I <sub>S</sub> =6A	-	-	1.2	V
Diode Forward Current (Note 2)	I <sub>S</sub>		-	-	6	A
Reverse Recovery Time	t <sub>rr</sub>	T <sub>J</sub> = 25°C, I <sub>F</sub> =5A di/dt = 100A/μs (Note3)	-	25	-	nS
Reverse Recovery Charge	Q <sub>rr</sub>		-	35	-	nC
Forward Turn-On Time	t <sub>on</sub>	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

**Notes:**

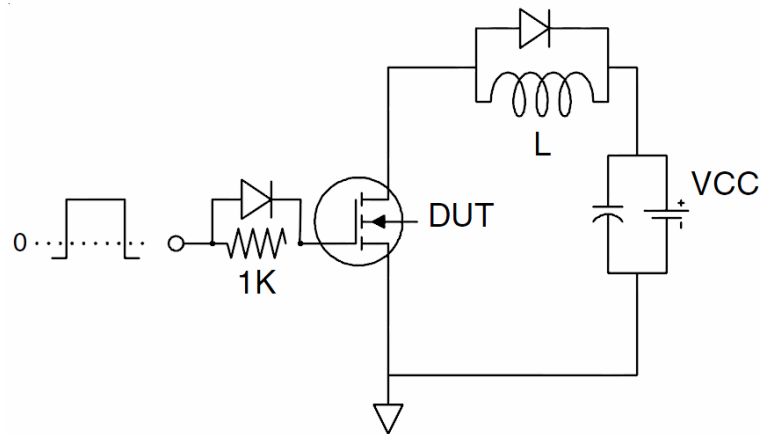
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, t ≤ 10 sec.
3. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
4. Guaranteed by design, not subject to production

### Test Circuit

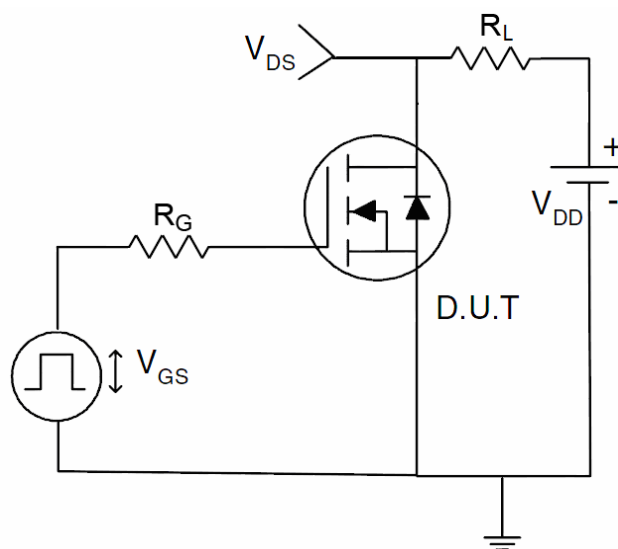
#### 1) $E_{AS}$ test Circuits



#### 2) Gate charge test Circuit



#### 3) Switch Time Test Circuit



Typical Electrical and Thermal Characteristics (Curves)

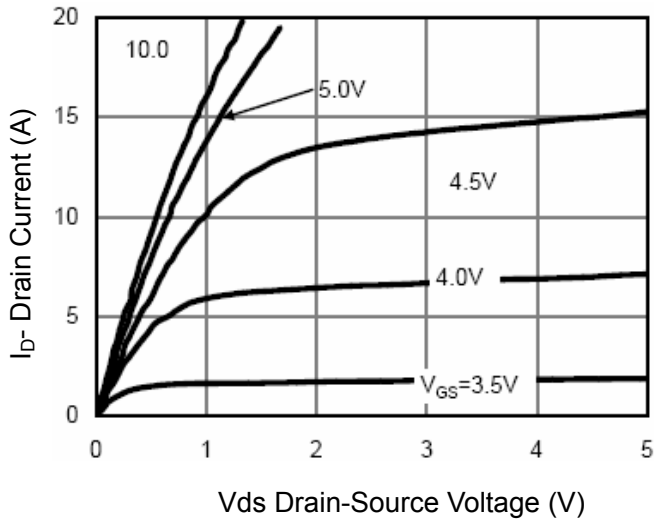


Figure 1 Output Characteristics

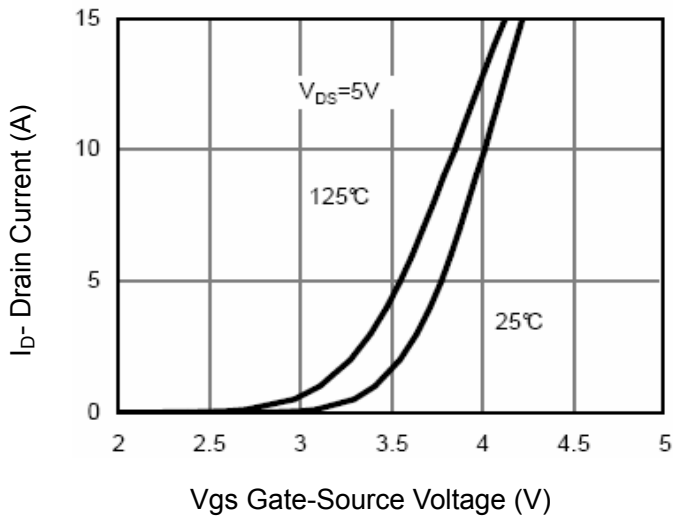


Figure 2 Transfer Characteristics

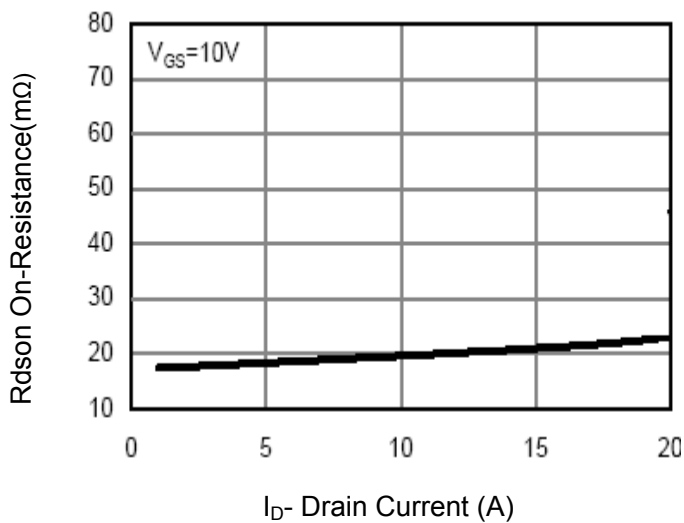


Figure 3 Rdson- Drain Current

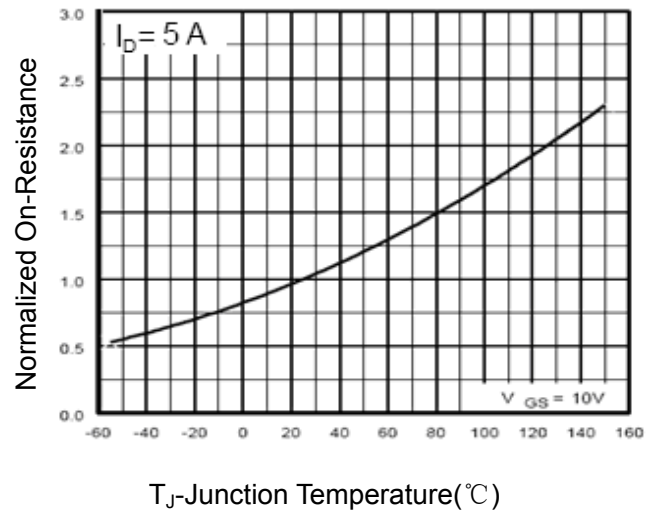


Figure 4 Rdson-Junction Temperature

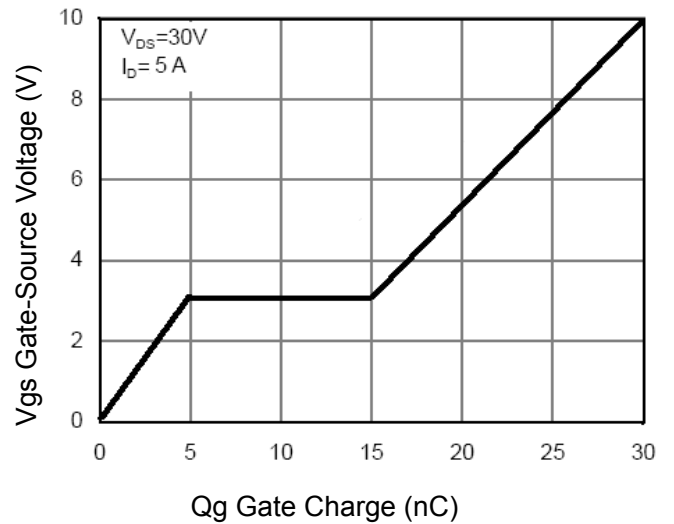


Figure 5 Gate Charge

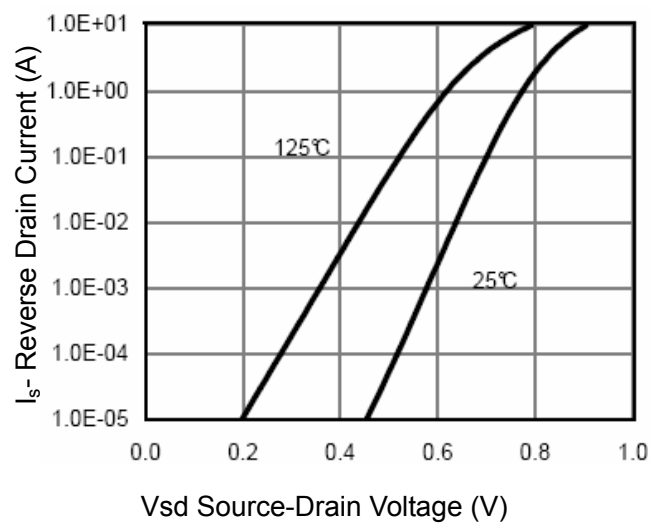


Figure 6 Source- Drain Diode Forward

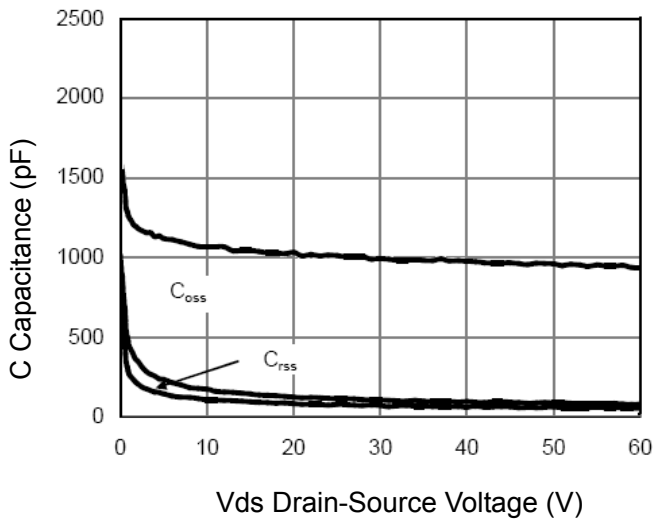


Figure 7 Capacitance vs Vds

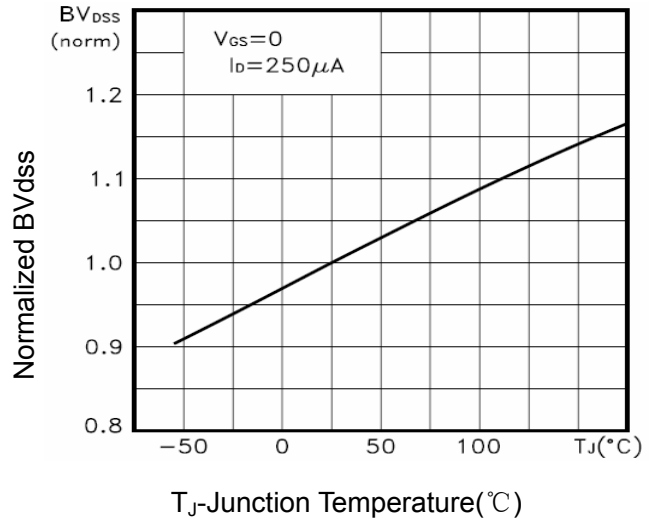


Figure 9  $BV_{DSS}$  vs Junction Temperature

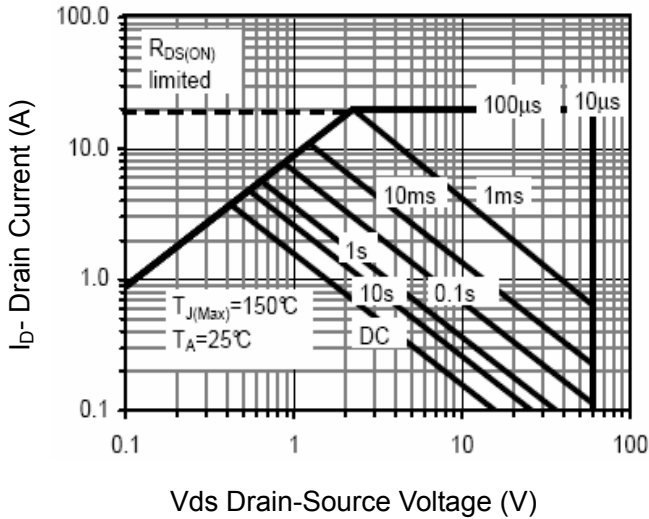


Figure 8 Safe Operation Area

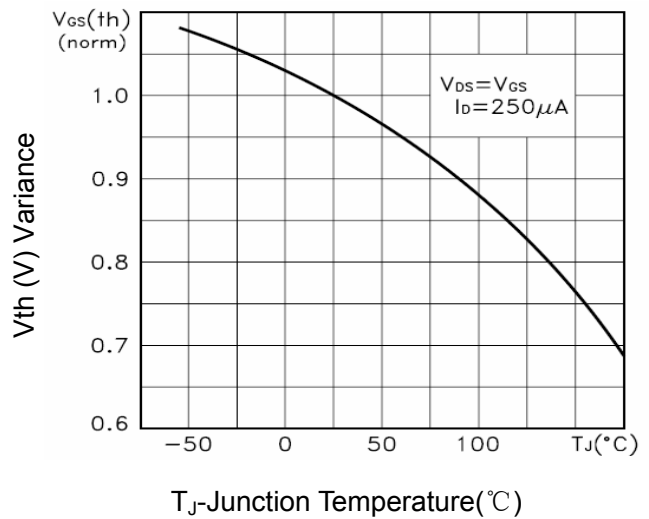


Figure 10  $V_{GS(th)}$  vs Junction Temperature

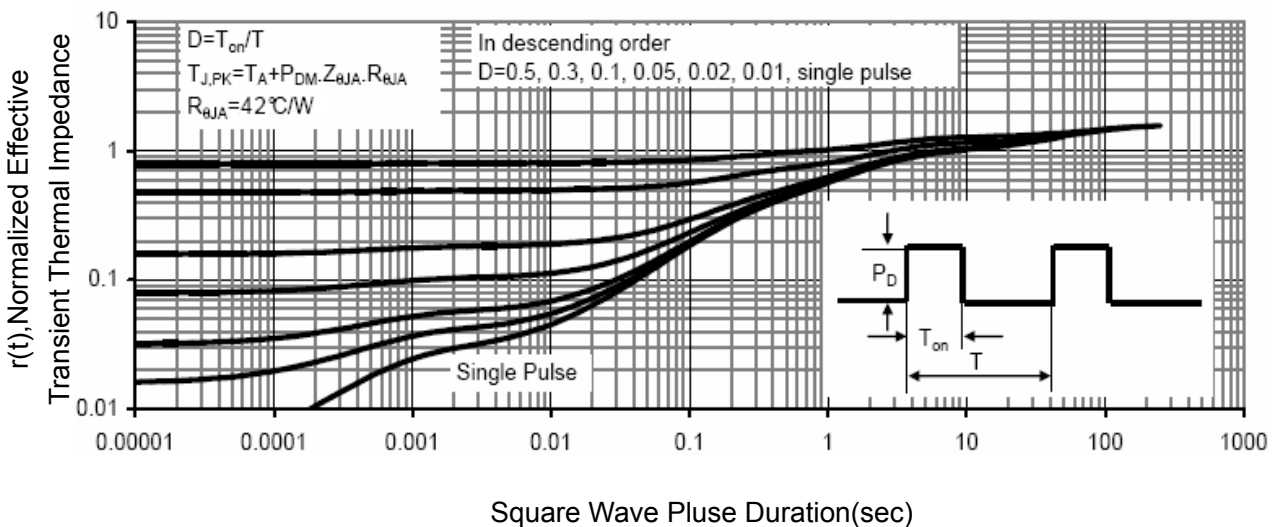
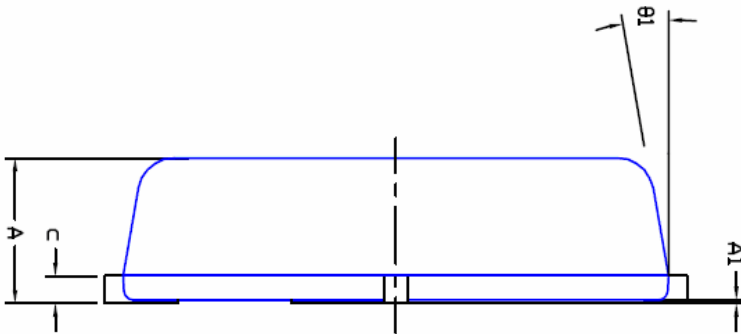
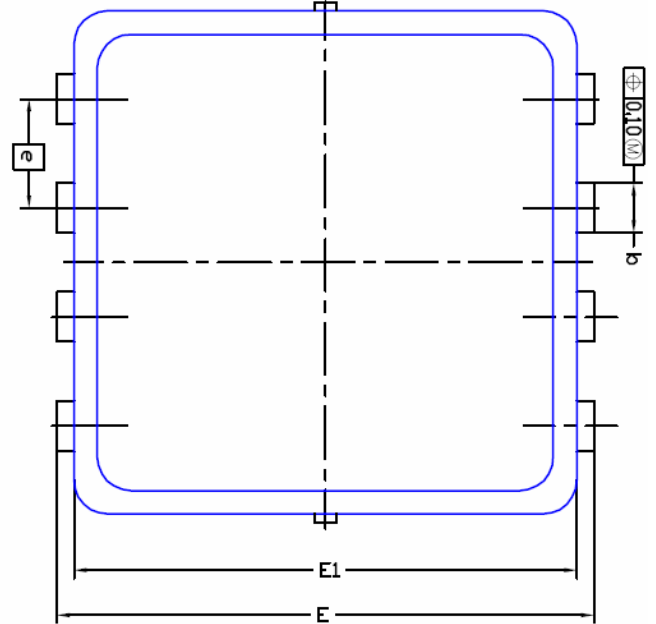
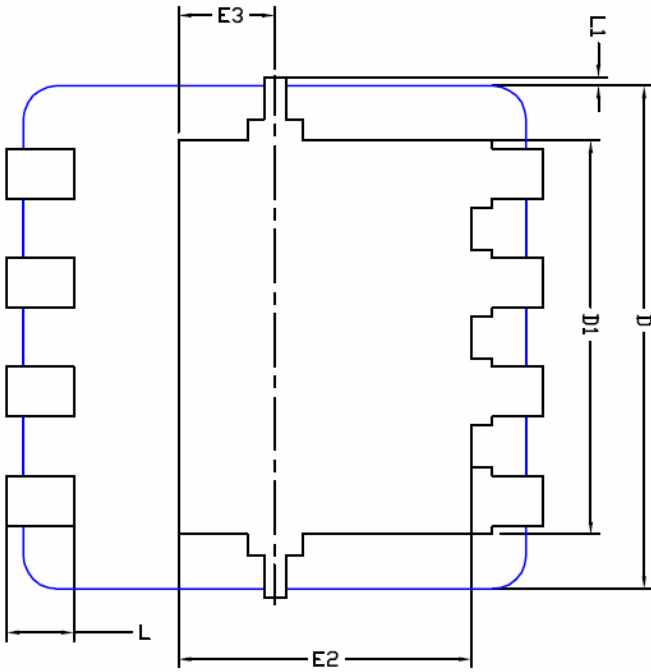


Figure 11 Normalized Maximum Transient Thermal Impedance

DFN3X3 EP Package Information



DIM.	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0,700	0,80	0,900	0,0276	0,0315	0,0354
A1	0,00	---	0,05	0,000	---	0,002
b	0,24	0,30	0,35	0,009	0,012	0,014
c	0,10	0,152	0,25	0,004	0,006	0,010
D	3,00 BSC			0,118 BSC		
D1	2,35 BSC			0,093 BSC		
E	3,20 BSC			0,126 BSC		
E1	3,00 BSC			0,118 BSC		
E2	1,75 BSC			0,069 BSC		
E3	0,575 BSC			0,023 BSC		
e	0,65 BSC			0,026 BSC		
L	0,30	0,40	0,50	0,0118	0,0157	0,0197
L1	0	---	0,100	0	---	0,004
θ1	0°	10°	12°	0°	10°	12°