

## N-Channel Enhancement Mode Power MOSFET

### Description

The HM25N03D uses advanced trench technology and design to provide excellent  $R_{DS(ON)}$  with low gate charge. It can be used in a wide variety of applications.

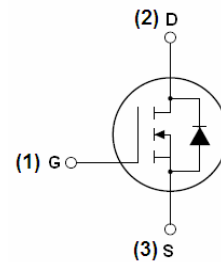
### General Features

- $V_{DS} = 30V, I_D = 25A$   
 $R_{DS(ON)} < 11m\Omega @ V_{GS} = 10V$   
 $R_{DS(ON)} < 16m\Omega @ V_{GS} = 5V$
- High density cell design for ultra low  $R_{dson}$
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high  $E_{AS}$
- Excellent package for good heat dissipation
- Special process technology for high ESD capability

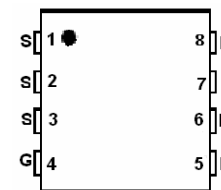
### Application

- Secondary side synchronous rectifier
- High side switch in POL DC/DC converter

**100% UIS TESTED!**



Schematic diagram



Marking and pin assignment

### Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
HM25N03D	HM25N03D	DFN 5x6 EP	-	-	-

### Absolute Maximum Ratings ( $T_C = 25^\circ C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DS}$	30	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Drain Current-Continuous	$I_D$	25	A
Pulsed Drain Current	$I_{DM}$	70	A
Maximum Power Dissipation	$P_D$	30	W
Derating factor		0.32	W/ $^\circ C$
Single pulse avalanche energy <sup>(Note 5)</sup>	$E_{AS}$	150	mJ
Operating Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 To 150	$^\circ C$

**Thermal Characteristic**

Thermal Resistance, Junction-to-Case <sup>(Note 2)</sup>	$R_{\theta JC}$	3.1	°C/W
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**Electrical Characteristics (TC=25°C unless otherwise noted)**

Parameter	Symbol	Condition	Min	Typ	Max	Unit
<b>Off Characteristics</b>						
Drain-Source Breakdown Voltage	$BV_{DSS}$	$V_{GS}=0V, I_D=250\mu A$	30	33	-	V
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS}=30V, V_{GS}=0V$	-	-	1	$\mu A$
Gate-Body Leakage Current	$I_{GSS}$	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	$\pm 100$	nA
<b>On Characteristics</b> <sup>(Note 3)</sup>						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	1	1.6	3	V
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=12A$	-	8	11	m $\Omega$
		$V_{GS}=5V, I_D=10A$	-	10	16	
Forward Transconductance	$g_{FS}$	$V_{DS}=10V, I_D=12A$	30	-	-	S
<b>Dynamic Characteristics</b> <sup>(Note 4)</sup>						
Input Capacitance	$C_{iss}$	$V_{DS}=15V, V_{GS}=0V,$ $F=1.0MHz$	-	1265	-	PF
Output Capacitance	$C_{oss}$		-	600	-	PF
Reverse Transfer Capacitance	$C_{rss}$		-	130	-	PF
<b>Switching Characteristics</b> <sup>(Note 4)</sup>						
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=15V, I_D=12A$ $V_{GS}=10V, R_{GEN}=6\Omega$	-	18	-	nS
Turn-on Rise Time	$t_r$		-	10	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	34	-	nS
Turn-Off Fall Time	$t_f$		-	10	-	nS
Total Gate Charge	$Q_g$	$V_{DS}=15V, I_D=12A,$ $V_{GS}=10V$	-	19	-	nC
Gate-Source Charge	$Q_{gs}$		-	2.7	-	nC
Gate-Drain Charge	$Q_{gd}$		-	2.5	-	nC
<b>Drain-Source Diode Characteristics</b>						
Diode Forward Voltage <sup>(Note 3)</sup>	$V_{SD}$	$V_{GS}=0V, I_S=12A$	-	0.85	1.2	V
Diode Forward Current <sup>(Note 2)</sup>	$I_S$		-	-	25	A
Reverse Recovery Time	$t_{rr}$	$T_J = 25^\circ C, I_F = 12A$ $di/dt = 100A/\mu s$ (Note3)	-	-	47	nS
Reverse Recovery Charge	$Q_{rr}$		-	-	25	nC
Forward Turn-On Time	$t_{on}$	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

**Notes:**

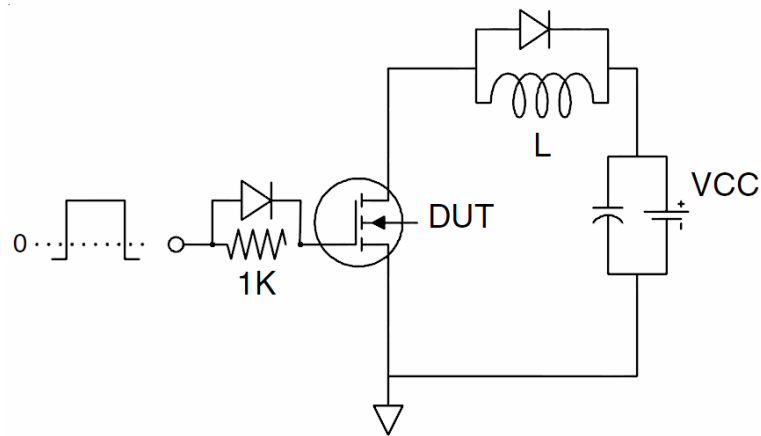
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board,  $t \leq 10$  sec.
3. Pulse Test: Pulse Width  $\leq 300\mu s$ , Duty Cycle  $\leq 2\%$ .
4. Guaranteed by design, not subject to production
5. EAS condition:  $T_J=25^\circ C, V_{DD}=15V, V_G=10V, L=0.1mH, R_g=25\Omega$

Test Circuit

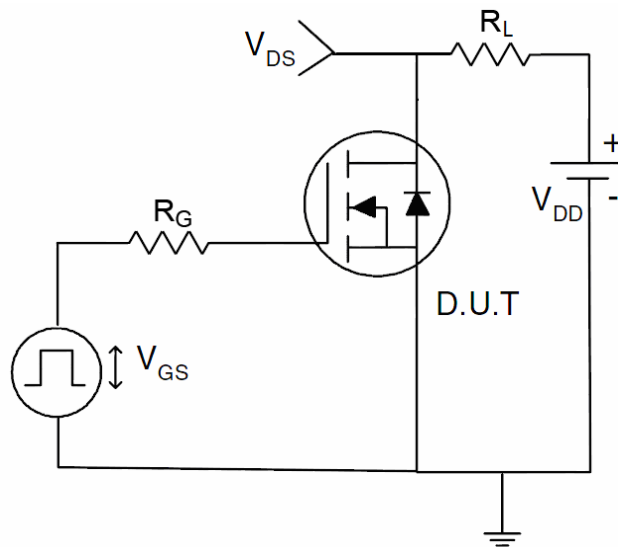
1)  $E_{AS}$  Test Circuits



2) Gate Charge Test Circuit



3) Switch Time Test Circuit



Typical Electrical and Thermal Characteristics (Curves)

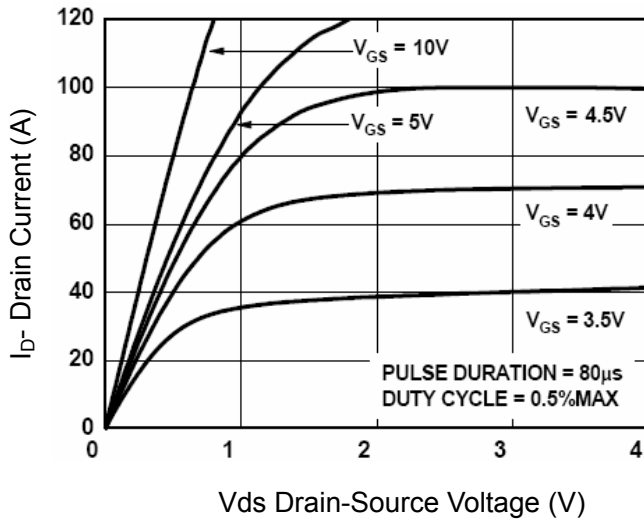


Figure 1 Output Characteristics

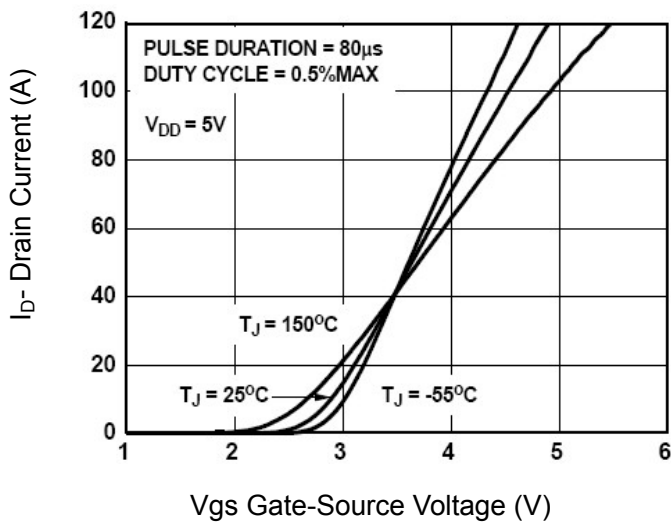


Figure 2 Transfer Characteristics

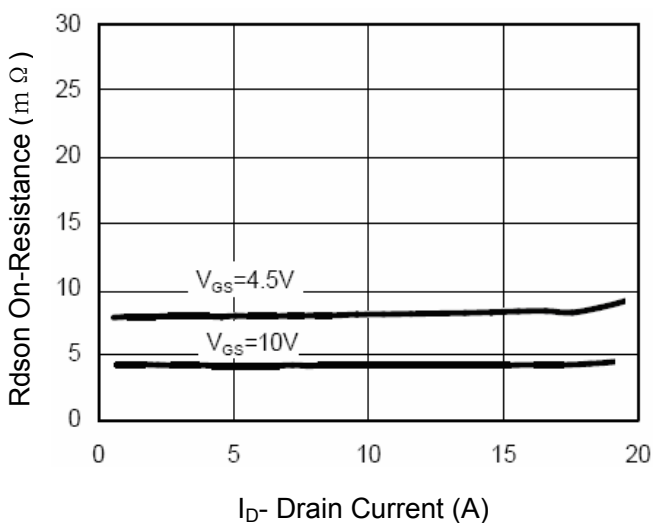


Figure 3 Rdson- Drain Current

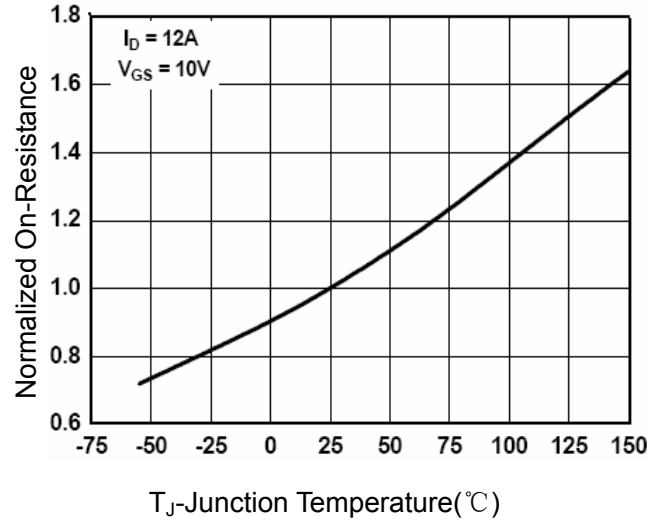


Figure 4 Rdson-Junction Temperature

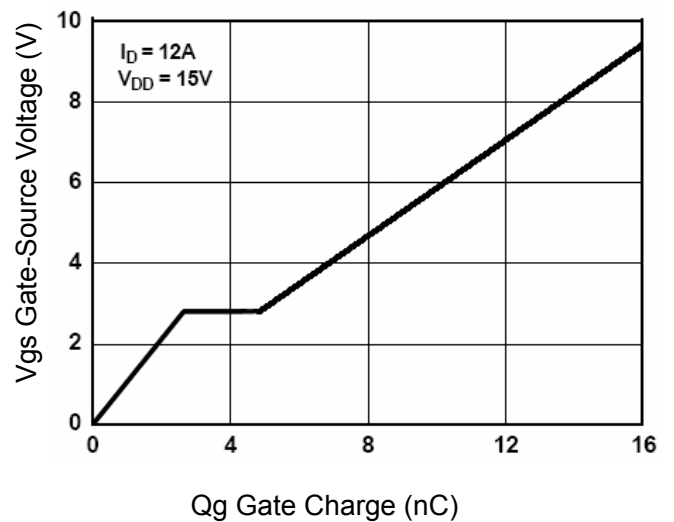


Figure 5 Gate Charge

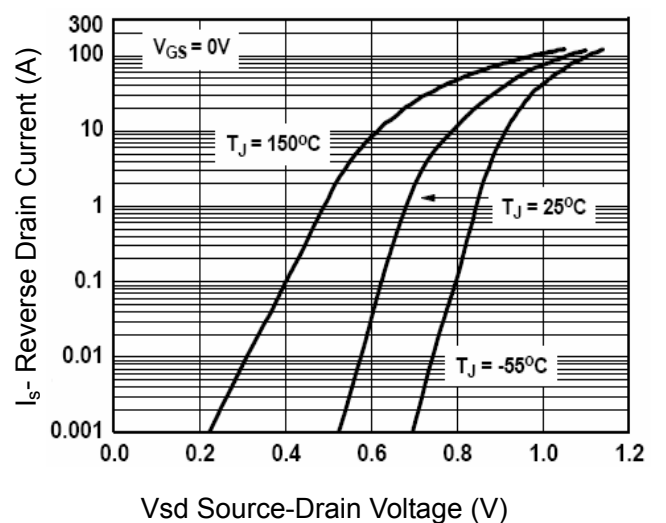


Figure 6 Source- Drain Diode Forward

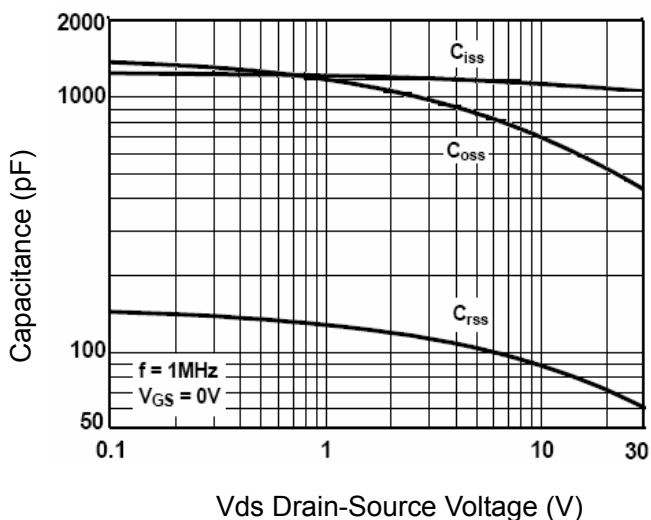


Figure 7 Capacitance vs Vds

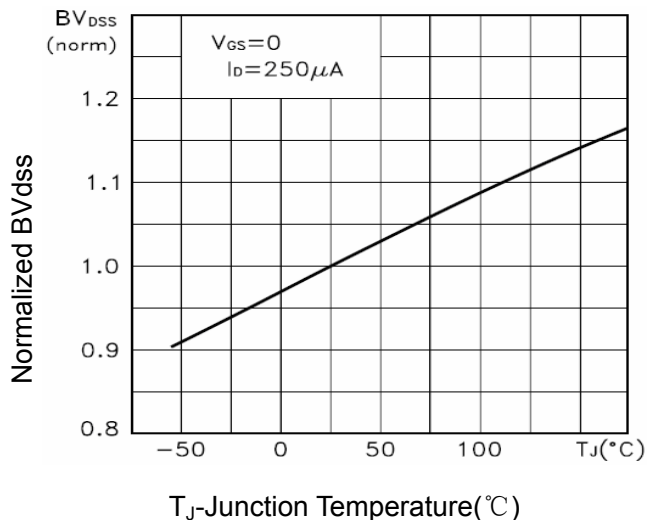


Figure 9  $BV_{DSS}$  vs Junction Temperature

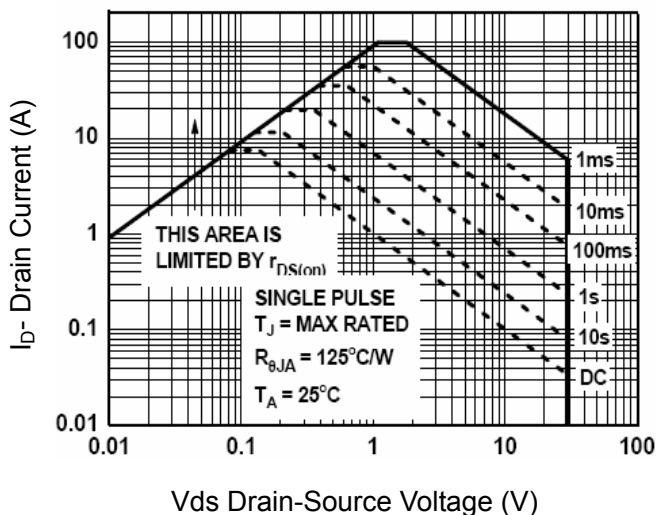


Figure 8 Safe Operation Area

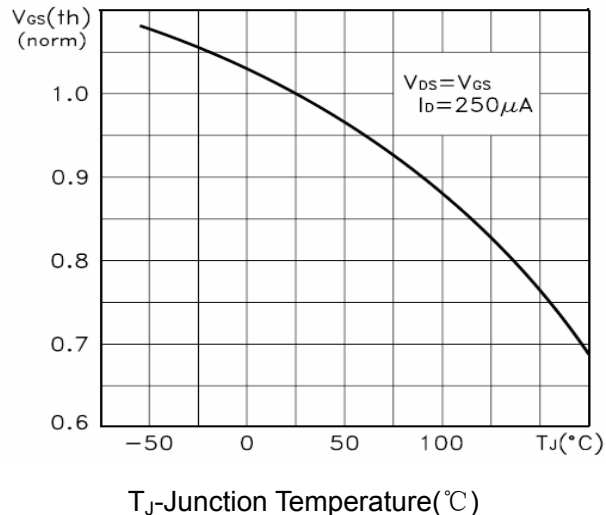


Figure 10  $V_{GS(th)}$  vs Junction Temperature

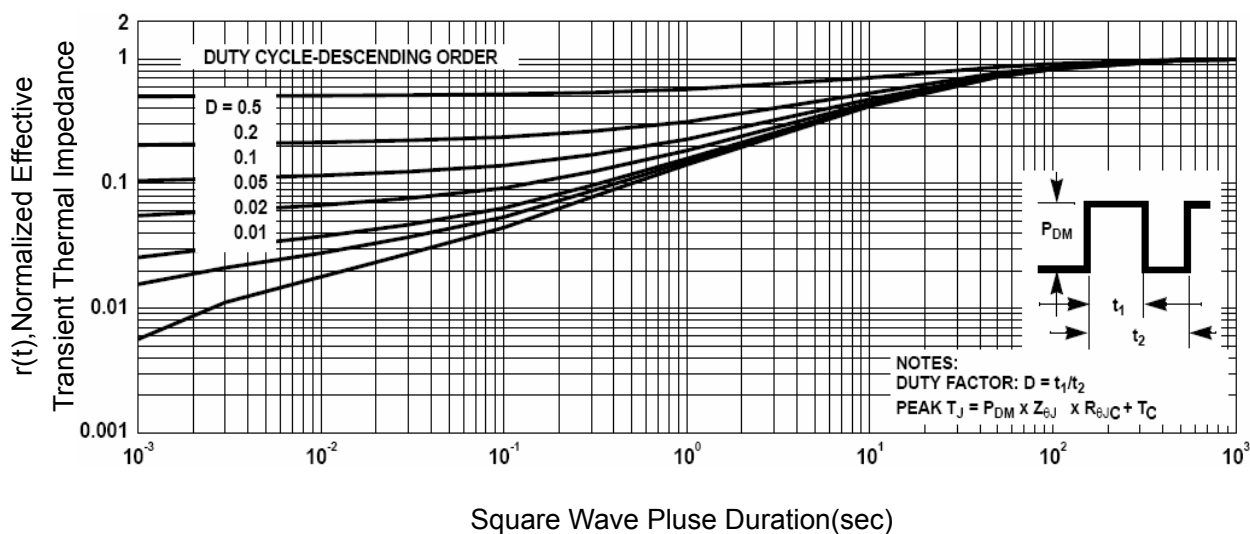
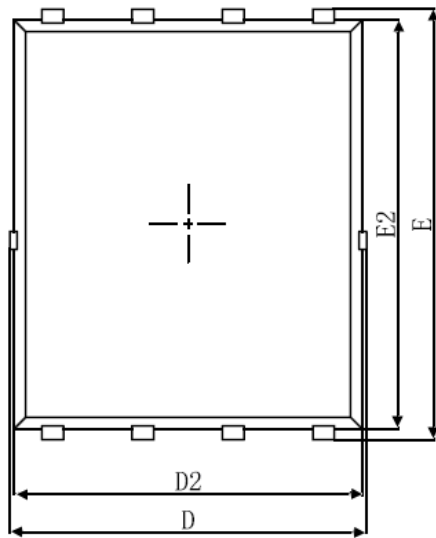
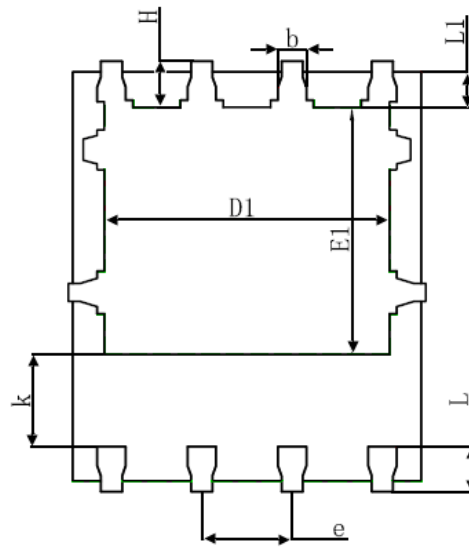


Figure 11 Normalized Maximum Transient Thermal Impedance

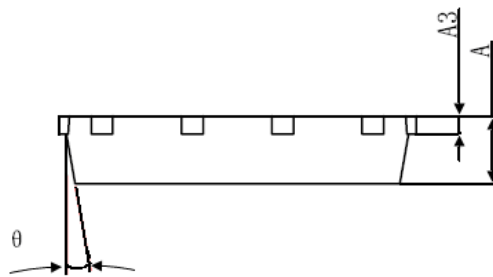
DFN5X6-8L Package Information



Top View  
[顶视图]



Bottom View  
[背视图]



Side View  
[侧视图]

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.900	1.000	0.035	0.039
A3	0.254REF.		0.010REF.	
D	4.944	5.096	0.195	0.201
E	5.974	6.126	0.235	0.241
D1	3.910	4.110	0.154	0.162
E1	3.375	3.575	0.133	0.141
D2	4.824	4.976	0.190	0.196
E2	5.674	5.826	0.223	0.229
k	1.190	1.390	0.047	0.055
b	0.350	0.450	0.014	0.018
e	1.270TYP.		0.050TYP.	
L	0.559	0.711	0.022	0.028
L1	0.424	0.576	0.017	0.023
H	0.574	0.726	0.023	0.029
θ	8°	12°	8°	12°