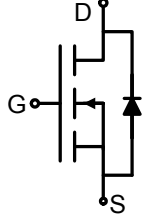
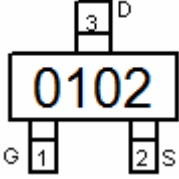



## N-Channel Enhancement Mode Power MOSFET

<p><b>Description</b> The HMGPFE0 uses advanced trench technology and design to provide excellent <math>R_{DS(ON)}</math> with low gate charge. It can be used in a wide variety of applications.</p> <p><b>General Features</b></p> <ul style="list-style-type: none"> <li>● <math>V_{DS} = 100V, I_D = 2A</math> <math>R_{DS(ON)} &lt; 240m\Omega @ V_{GS}=10V</math> (Typ:210m<math>\Omega</math>)</li> <li>● High density cell design for ultra low Rds on</li> <li>● Fully characterized avalanche voltage and current</li> <li>● Excellent package for good heat dissipation</li> </ul> <p><b>Application</b></p> <ul style="list-style-type: none"> <li>● Power switching application</li> <li>● Hard switched and high frequency circuits</li> <li>● Uninterruptible power supply</li> </ul>	 <p>Schematic diagram</p>  <p>Marking and pin assignment</p>  <p>SOT-23 top view</p>
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### Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
0102	HMGPFE0	SOT-23	Ø330mm	12mm	2500 units

### Absolute Maximum Ratings ( $T_A=25^\circ C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DS}$	100	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Drain Current-Continuous	$I_D$	2	A
Drain Current-Pulsed <sup>(Note 1)</sup>	$I_{DM}$	5	A
Maximum Power Dissipation	$P_D$	1.25	W
Operating Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 To 150	$^\circ C$

### Thermal Characteristic

Thermal Resistance, Junction-to-Ambient <sup>(Note 2)</sup>	$R_{\theta JA}$	100	$^\circ C/W$
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### Electrical Characteristics ( $T_A=25^\circ C$ unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
<b>Off Characteristics</b>						
Drain-Source Breakdown Voltage	$BV_{DSS}$	$V_{GS}=0V, I_D=250\mu A$	100	110	-	V
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS}=100V, V_{GS}=0V$	-	-	1	$\mu A$

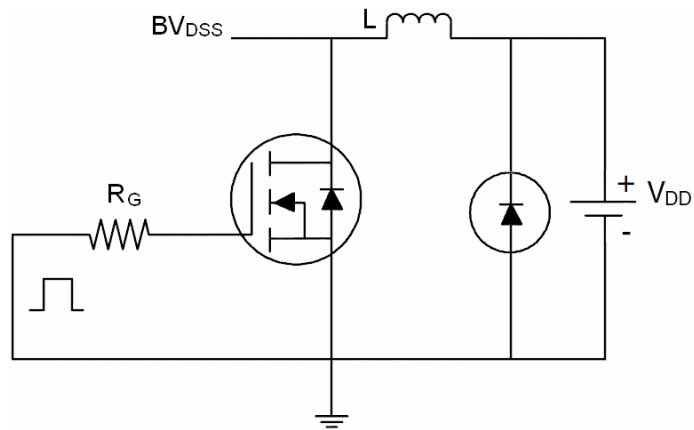
Gate-Body Leakage Current	$I_{GSS}$	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	$\pm 100$	nA
<b>On Characteristics</b> (Note 3)						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	1.2	1.8	2.5	V
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=1A$	-	210	240	m $\Omega$
Forward Transconductance	$g_{FS}$	$V_{DS}=5V, I_D=1A$	1	-	-	S
<b>Dynamic Characteristics</b> (Note 4)						
Input Capacitance	$C_{iss}$	$V_{DS}=50V, V_{GS}=0V,$ $F=1.0MHz$	-	190	-	PF
Output Capacitance	$C_{oss}$		-	22	-	PF
Reverse Transfer Capacitance	$C_{rss}$		-	13	-	PF
<b>Switching Characteristics</b> (Note 4)						
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=50V, I_D=1.3A, R_L=39\Omega$ $V_{GS}=10V, R_G=1\Omega$	-	6	-	nS
Turn-on Rise Time	$t_r$		-	10	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	10	-	nS
Turn-Off Fall Time	$t_f$		-	6	-	nS
Total Gate Charge	$Q_g$	$V_{DS}=50V, I_D=1.3A,$ $V_{GS}=10V$	-	5.2	-	nC
Gate-Source Charge	$Q_{gs}$		-	0.75	-	nC
Gate-Drain Charge	$Q_{gd}$		-	1.4	-	nC
<b>Drain-Source Diode Characteristics</b>						
Diode Forward Voltage (Note 3)	$V_{SD}$	$V_{GS}=0V, I_S=1.3A$	-	-	1.2	V
Diode Forward Current (Note 2)	$I_S$		-	-	2	A

**Notes:**

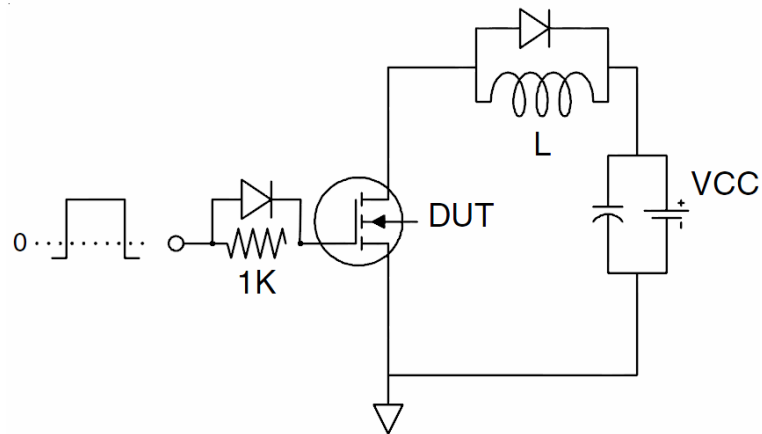
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board,  $t \leq 10$  sec.
3. Pulse Test: Pulse Width  $\leq 300\mu s$ , Duty Cycle  $\leq 2\%$ .
4. Guaranteed by design, not subject to production

### Test Circuit

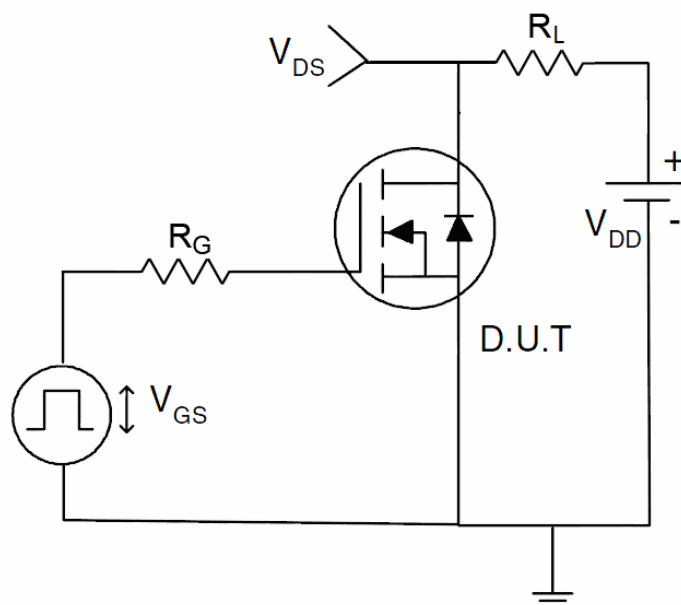
#### 1) $E_{AS}$ test circuit



#### 2) Gate charge test circuit



#### 3) Switch Time Test Circuit



Typical Electrical and Thermal Characteristics (Curves)

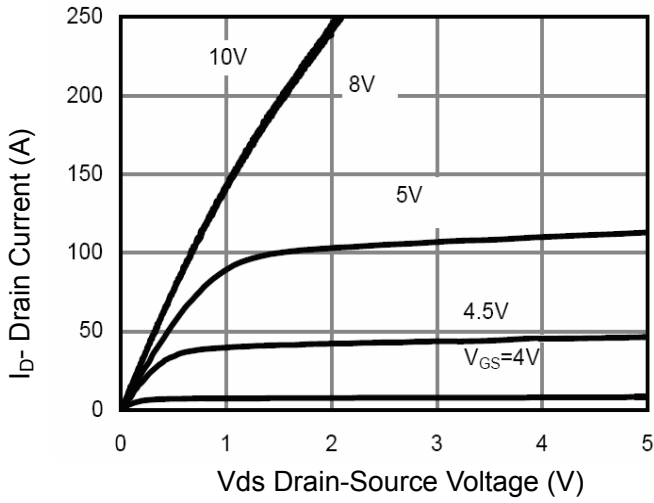


Figure 1 Output Characteristics

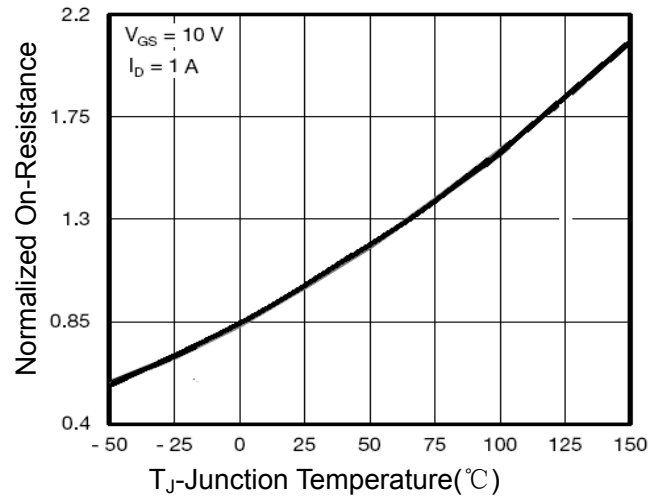


Figure 4  $R_{ds(on)}$ -Junction Temperature

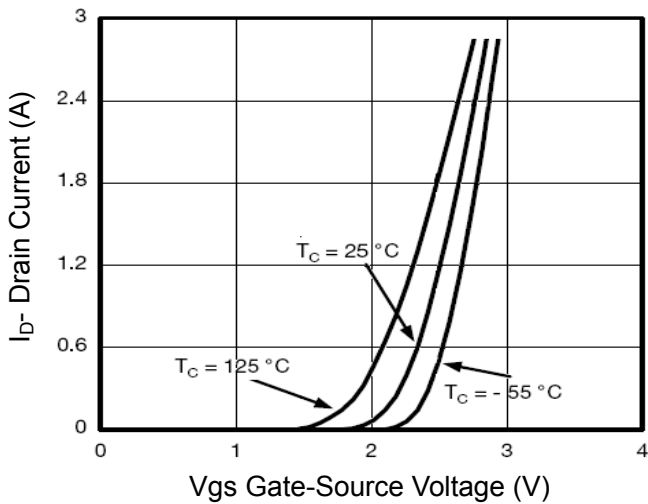


Figure 2 Transfer Characteristics

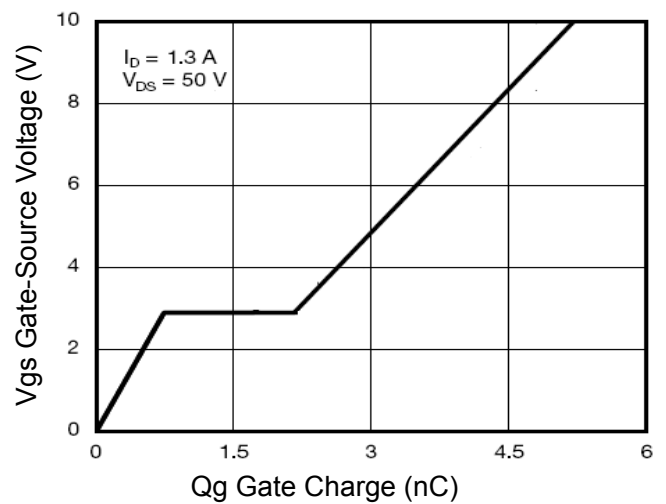


Figure 5 Gate Charge

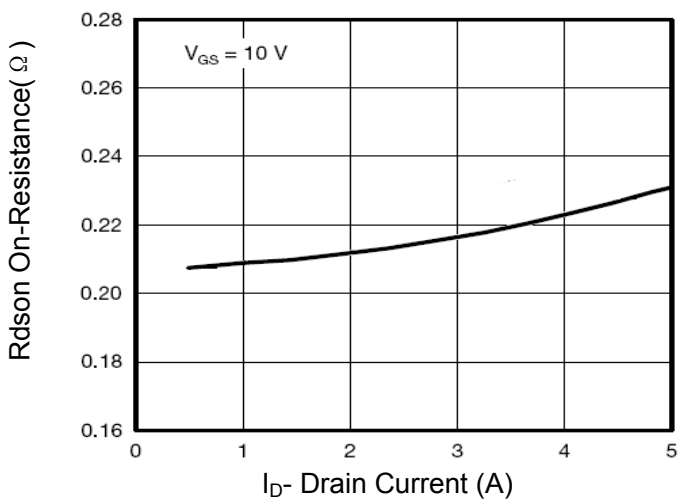


Figure 3  $R_{ds(on)}$ - Drain Current

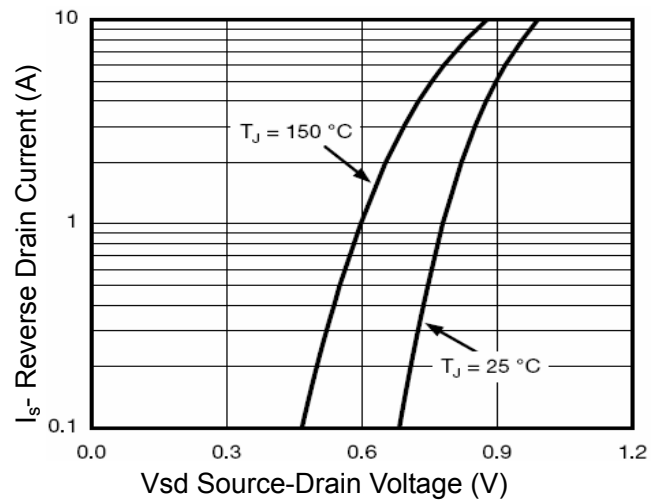


Figure 6 Source- Drain Diode Forward

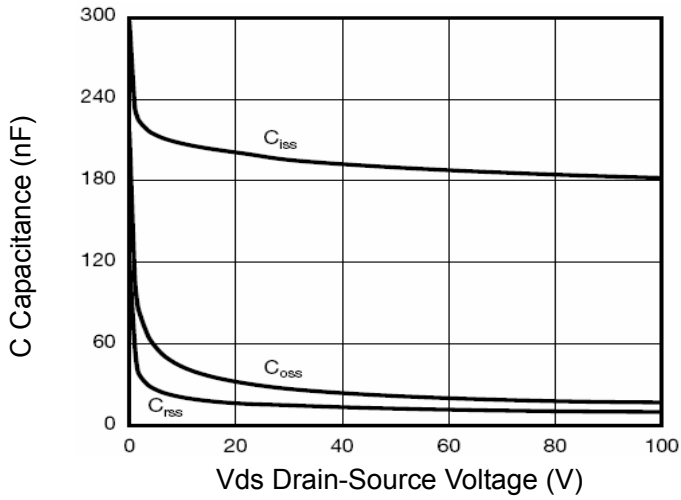


Figure 7 Capacitance vs Vds

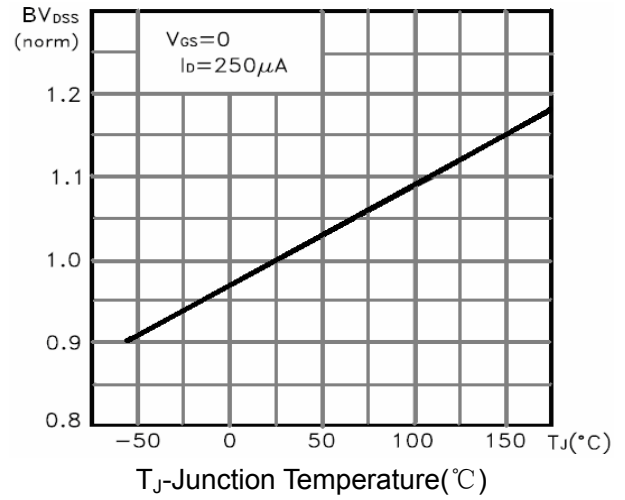


Figure 9  $BV_{DSS}$  vs Junction Temperature

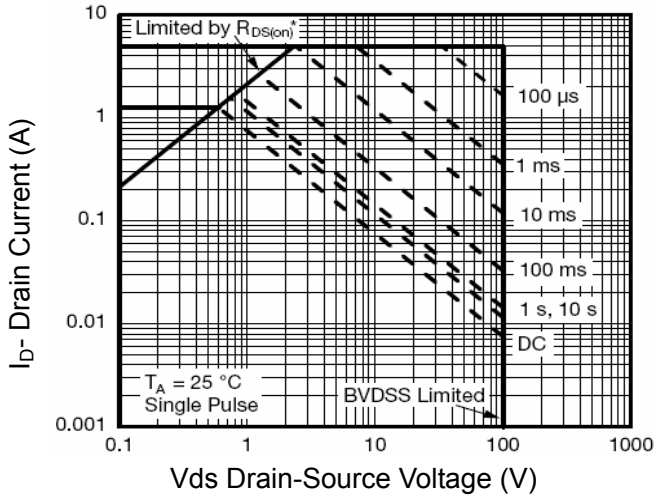


Figure 8 Safe Operation Area

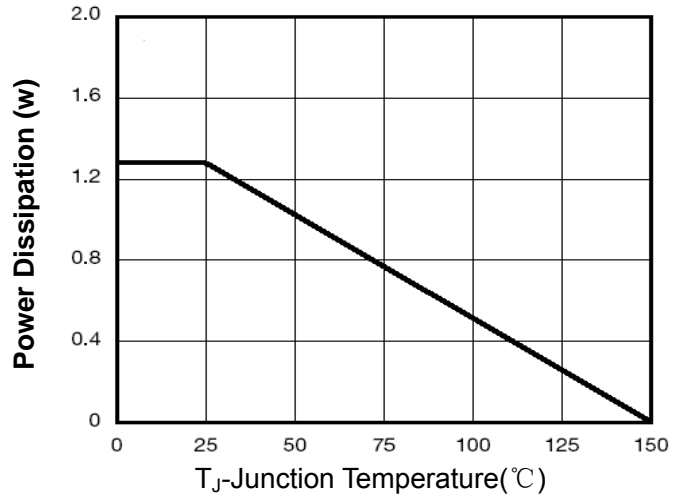


Figure 10 Power De-ratin

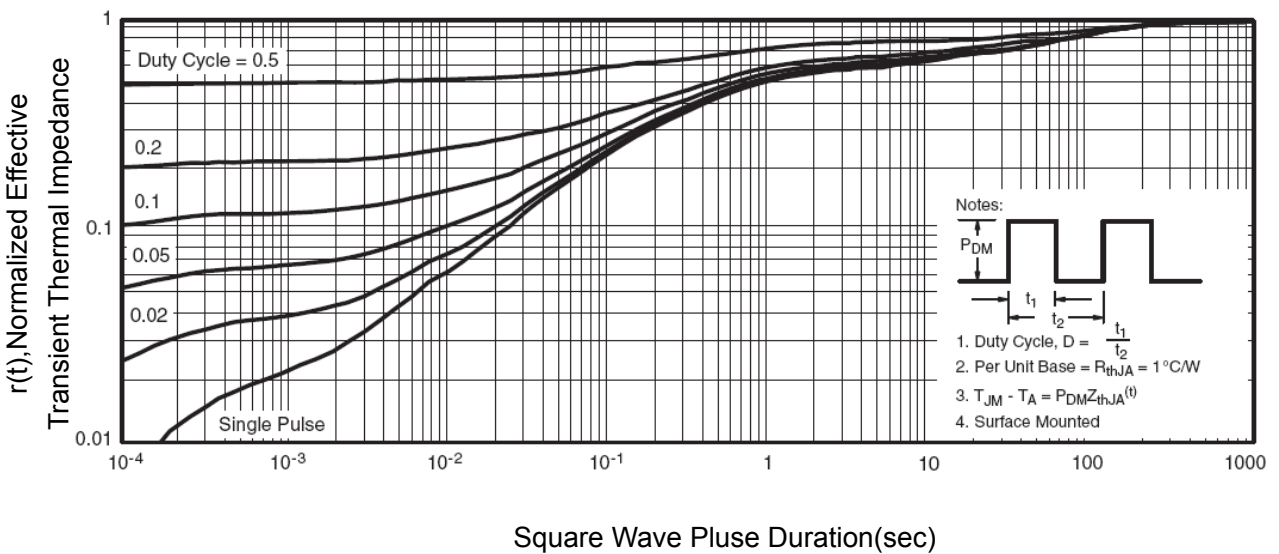
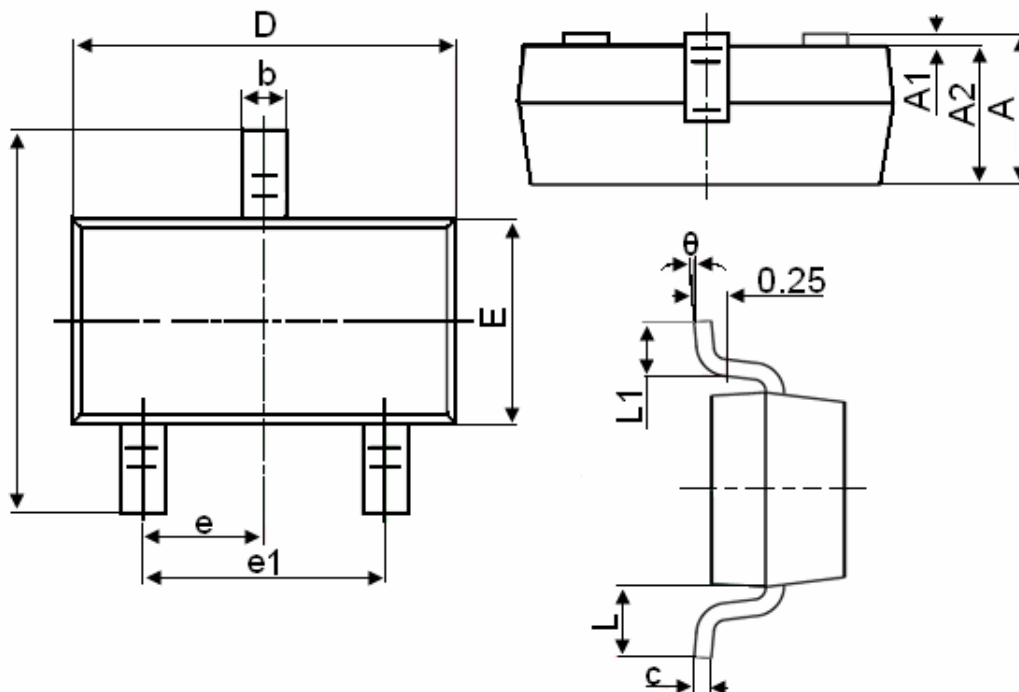


Figure 11 Normalized Maximum Transient Thermal Impedance

SOT-23 Package Information



Symbol	Dimensions in Millimeters	
	MIN.	MAX.
A	0.900	1.150
A1	0.000	0.100
A2	0.900	1.050
b	0.300	0.500
c	0.080	0.150
D	2.800	3.000
E	1.200	1.400
E1	2.250	2.550
e	0.950TYP	
e1	1.800	2.000
L	0.550REF	
L1	0.300	0.500
$\theta$	0°	8°

Notes

1. All dimensions are in millimeters.
2. Tolerance  $\pm 0.10\text{mm}$  (4 mil) unless otherwise specified
3. Package body sizes exclude mold flash and gate burrs. Mold flash at the non-lead sides should be less than 5 mils.
4. Dimension L is measured in gauge plane.
5. Controlling dimension is millimeter, converted inch dimensions are not necessarily exact.